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Sir:

Transmitted herewith for filing is the patent application of

Inventor(s): Shigeyuki UEDA

For: SEMICONDUCTOR CHIP AND METHOD OF PRODUCTING THE SAME

Enclosed are:

☒ Specification and Claim(s).

☒ Oath or Declaration (executed).

☒ 1 sheet(s) of drawings (2 sets).

☒ An assignment of the invention to ROHM CO., LTD.

☐ Copy of _____ priority application(s).

☐ Preliminary Amendment

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INDEP. CLAIMS	4-3	1	X $39 $78	$78
Fee for Multiple Dependent Claims $130/$260				0
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SEMICONDUCTOR CHIP AND METHOD OF PRODUCING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor chip and a method of producing the same.

Description of Related Art

Internal wiring in a semiconductor chip is generally composed of aluminum or the like in order to hold down the production cost. The wiring composed of aluminum or the like is subjected to oxidation by moisture. Therefore, a surface of the wiring is covered with a surface protective film composed of silicon nitride, for example. An opening is formed on the surface protective film to expose a part of the wiring, thereby forming a pad for external connection used for connection to an external terminal such as a lead terminal. An end of a wire composed of gold (Au), for example, is made to adhere and connected to the external connection pad, and the other end of the wire is connected to the external terminal, thereby achieving electrical connection between the wiring in the semiconductor chip and the external terminal.

After the wire is connected to the external connection pad, it is preferable that the surface of

the pad is completely covered with the wire. When the adhesion area of the wire on the external connection pad is small, however, the surface of the pad is not completely covered with the wire, so that a part of the pad may remain exposed. Because the pad is composed of aluminum or the like, if the pad is exposed, it may be oxidized by moisture or the like and corroded.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor chip in which a pad for external connection may not be corroded irrespective of a connected state of a wire and a method of producing the same.

Another object of the present invention is to provide a semiconductor device having a chip-on-chip structure using the above-mentioned semiconductor chip and a method of producing the same.

A semiconductor chip according to the present invention comprises a surface protective film for covering internal wiring; an external connection pad which is formed by partially exposing the internal wiring from the surface protective film; and a wire connecting portion which is formed using a metal material having oxidation resistance on the external connection pad and to which a wire for electrical

connection to an external terminal is connected.

According to the present invention, the wire connecting portion composed of a metal material having oxidation resistance is formed on the external connection pad. In other words, the surface of the external connection pad is covered with the wire connecting portion composed of the metal material having oxidation resistance. Consequently, the external connection pad is not exposed to the exterior irrespective of a connected state of the wire to the wire connecting portion. Accordingly, the external connection pad may not be oxidized by moisture or the like and corroded.

The semiconductor chip may be overlapped with and joined to a surface of another solid device (for example, another semiconductor chip) in a state where the surface protective film is opposed to a surface of the solid device. In this case, it is preferable that the semiconductor chip further comprises an internal connection (chip connecting pad) which is formed by partially exposing the internal wiring from the surface protective film in a portion different from the external connection pad, and a bump formed in a raised state on the internal connection pad (chip connecting pad) using a metal material having oxidation

resistance in order to make electrical connection to the solid device.

Furthermore, in this case, it is preferable that the wire connecting portion is composed of the same material as that for the bump. Consequently, it is possible to form the wire connecting portion at the same step as the bump.

A method of producing a semiconductor device according to the present invention is a method of producing a semiconductor chip which is to be overlapped with and joined to a surface of another solid device (for example, another semiconductor chip), comprising the steps of stacking a surface protective film on internal wiring; forming an opening on the surface protective film to partially expose the internal wiring, to form an external connection pad and an internal connection pad (chip connecting pad); and selectively plating (preferably, plating with a material having oxidation resistance) the external connection pad and the internal connection pad (chip connecting pad), to respectively form a wire connecting portion to which a wire for electrical connection to an external terminal is connected and a bump for electrical connection to the other semiconductor chip.

According to the method, the wire connecting portion can be formed at the same step as the bump. Accordingly, the number of steps of producing the semiconductor chip is not increased by providing the wire connecting portion on the external connection pad.

It is preferable that the wire connecting portion is composed of the same material as that for the wire. Consequently, it is possible to improve the adhesive properties of the wire to the wire connecting portion.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an illustrative sectional view showing the schematic structure of a semiconductor device to which a semiconductor chip according to an embodiment of the present invention is applied; and

Fig. 2 is a cross-sectional view showing a part of a primary chip provided in the semiconductor device shown in Fig. 1 in enlarged fashion.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is an illustrative sectional view showing

the schematic structure of a semiconductor device to which a semiconductor chip according to an embodiment of the present invention is applied. The semiconductor device has a so-called chip-on-chip structure, and is constructed by overlapping and joining a secondary chip 2 with and to a surface 11 of a primary chip 1, and containing the primary chip 1 and the secondary chip 2 in a package 3.

The primary chip 1 and the secondary chip 2 are composed of silicon, for example. The surface 11 of the primary chip 1 is a surface, on the side of an active surface layer region where a functional device such as a transistor is formed, of a semiconductor substrate forming a base body of the primary chip 1. The forefront of the surface 11 is covered with a surface protective film (not shown) composed of silicon nitride, for example. On the surface protective film, a plurality of wire connecting portions 12 are arranged in the vicinity of its peripheral edge. The wire connecting portion 12 is connected to a lead frame 5 by a bonding wire 4 composed of gold, for example. Further, a plurality of bumps BM for electrical connection to the secondary chip 2 are arranged on the surface 11 of the primary chip 1.

The secondary chip 2 is joined to the primary chip

1 in a so-called face-down method in which a surface 21 of the secondary chip 2 is opposed to the surface 11 of the primary chip 1. The surface 21 of the secondary chip 2 is a surface, on the side of an active surface layer region where a functional device such as a transistor is formed, of a semiconductor substrate forming a base body of the secondary chip 2. The forefront of the surface 21 is covered with a surface protective film (not shown) composed of silicon nitride, for example. On the surface protective film, a plurality of bumps BS connected to internal wiring are arranged opposite to the bumps BM on the primary chip 1. The bumps BS on the secondary chip 2 are respectively connected to the opposite bumps BM on the primary chip 1. Consequently, the secondary chip 2 is supported with predetermined spacing held from the surface 11 of the primary chip 1, and is electrically connected to the primary chip 1.

Fig. 2 is a cross-sectional view showing a part of the primary chip 1 in enlarged fashion. On a semiconductor substrate 13 forming a base body of the primary chip 1, an interlayer insulating film 14 composed of silicon oxide, for example, is formed. Internal wiring 15 composed of aluminum, for example, is disposed on the interlayer insulating film 14.

Surfaces of the interlayser insulating film 14 and the internal wiring 15 are covered with a surface protective film 16 composed of silicon nitride, for example. Openings 17A and 17B are formed on the surface protective film 16 to partially expose the internal wiring 15 from the surface protective film 16, thereby respectively forming an inter-chip connecting pad 15A and a pad for external connection 15B.

On the inter-chip connecting pad 15A formed in the opening 17A, the bump BM composed of a metal having oxidation resistance is formed in a raised state. On the other hand, the external connection pad 15B is formed at a peripheral edge of the primary chip 1. On the external connection pad 15B, the wire connecting portion 12 for connecting the bonding wire 4 (see Fig. 1) is formed in a raised state using a metal having oxidation resistance.

Examples of the metal having oxidation resistance composing the bump BM and the wire connecting portion 12 include gold, platinum, silver, palladium, and iridium. Particularly, gold is preferably used. It is preferable that the wire connecting portion 12 is composed of the same material as that for the bonding wire 4. Consequently, it is possible to improve the adhesive properties of the

bonding wire 4 to the wire connecting portion 12.

Furthermore, the bump BM and the wire connecting portion 12 can be formed at the same step using the same material. For example, the openings 17A and 17B are formed on the surface protective film 16, and a seed film is then formed on the surface protective film 16 having the openings 17A and 17B formed thereon. The pattern of a resist film having openings corresponding to the inter-chip connecting pad 15A (the opening 17A) and the external connection pad 15B (the opening 17B) is formed on the seed film, followed by plating with a material for the bump BM and the wire connecting portion 12. Thereafter, the resist film on the seed film is removed, and the seed film exposed by removing the resist film is then removed. Consequently, the bump BM and the wire connecting portion 12 can be respectively obtained on the inter-chip connecting pad 15A and the external connection pad 15B.

As described in the foregoing, according to the present embodiment, the wire connecting portion 12 composed of a metal material having oxidation resistance is formed in a raised state on the external connection pad 15B (wiring 15). In other words, a surface of the external connection pad 15B is covered with the wire connecting portion 12 composed of the

metal material having oxidation resistance. The bonding wire for electrical connection to the lead frame 5 is welded to the wire connecting portion 12. Consequently, the external connection pad 15B is not exposed to the exterior irrespective of a connected state of the bonding wire 4 to the wire connecting portion 12. Accordingly, the external connection pad 15B may not be oxidized by moisture or the like and corroded.

Furthermore, the wire connecting portion 12 can be formed at the same step as the bump BM by using the same material as that for the bump BM. Even though the wire connecting portion 12 is provided, therefore, the number of steps of producing the primary chip 1 is not increased. However, the bump BM and the wire connecting portion 12 may be respectively composed of different materials. In this case, the wire connecting portion 12 is formed at a step different from the bump BM.

Although description has been made of an embodiment of the present invention, the present invention can be embodied in another embodiment. Although both the primary chip 1 and the secondary chip 2 are chips composed of silicon, for example, they may be semiconductor chips using another arbitrary

semiconductor material such as a compound semiconductor (for example, a gallium arsenic semiconductor) or a germanium semiconductor in addition to silicon. In this case, a semiconductor material for the primary chip 1 and a semiconductor material for the secondary chip 2 may be the same or different from each other.

Although in the above-mentioned embodiment, the semiconductor device having a chip-on-chip structure is taken as an example, the semiconductor chip according to the present invention is widely applicable to a semiconductor device having a structure other than the chip-on-chip structure.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

The application is based on Japanese Patent Application Serial No. 11-265744 filed with the Japanese Patent Office on September 20, 1999, the content of which is incorporated hereinto by reference.

What is Claimed is:

1. A semiconductor chip, comprising:

a surface protective film for covering internal wiring;

an external connection pad which is formed by partially exposing said internal wiring from the surface protective film; and

a wire connecting portion which is formed using a metal material having oxidation resistance on the external connection pad and to which a wire for electrical connection to an external terminal is connected.

2. The semiconductor chip according to claim 1, wherein

said semiconductor chip is overlapped with and joined to a surface of another solid device in a state where said surface protective film is opposed to a surface of the solid device.

3. The semiconductor chip according to claim 2, further comprising

an internal connection pad which is formed by partially exposing said internal wiring from said surface protective film in a portion different from said external connection pad, and

a bump formed in a raised state on the internal

connection pad using a metal material having oxidation resistance in order to make electrical connection to said solid device.

4. The semiconductor chip according to claim 2, wherein

said solid device includes another semiconductor chip.

5. The semiconductor chip according to claim 1, wherein

said wire connecting portion is composed of the same material as that for said bump.

6. A semiconductor device having a chip-on-chip structure in which a secondary chip is overlapped with and joined to a surface of a primary chip, wherein

said primary chip comprises

a surface protective film for covering internal wiring,

an external connection pad formed by partially exposing the internal wiring from the surface protective film,

a wire connecting portion which is formed using a metal material having oxidation resistance on the external connection pad and to which a wire for electrical connection to an external terminal is connected,

an internal connection pad which is formed by partially exposing said internal wiring from said surface protective film in a portion different from said external connection pad, and

a bump which is formed in a raised state on the internal connection pad using a metal material having oxidation resistance for electrically connecting the primary chip and the secondary chip.

7. The semiconductor device according to claim 6, wherein

said wire connecting portion is composed of the same material as that for said bump.

8. A method of producing a semiconductor chip which is to be overlapped with and joined to a surface of another solid device, comprising the steps of:

stacking a surface protective film on internal wiring;

forming an opening on the surface protective film to partially expose said internal wiring, to form an external connection pad and an internal connection pad; and

selectively plating said external connection pad and the internal connection pad, to respectively form a wire connecting portion to which a wire for electrical connection to an external terminal is

connected and a bump for electrical connection to the other solid device.

9. A method of producing a semiconductor device having a chip-on-chip structure in which a secondary chip is overlapped with and joined to a surface of a primary chip, comprising the steps of:

stacking a surface protective film on internal wiring in the primary chip;

forming an opening on said surface protective film to partially expose said internal wiring, to form an external connection and an internal connection;

and

selectively plating said external connection pad and the internal connection pad, to respectively form a wire connecting portion to which a wire for electrical connection to an external terminal is connected and a bump for electrical connection to said secondary chip; and

joining the primary chip and the secondary chip to each other through said bump.

ABSTRACT OF THE DISCLOSURE

A semiconductor chip which is to be overlapped with and joined to a surface of another solid device. The semiconductor chip has a surface protective film for covering internal wiring, an external connection pad which is formed by partially exposing the internal wiring from the surface protective film, and a wire connecting portion which is formed using a metal material having oxidation resistance on the external connection pad and to which a wire for electrical connection to an external terminal is connected. It is preferable that the semiconductor chip further has an internal connection pad used for connection to the solid device and a bump formed on the pad.

FIG.1

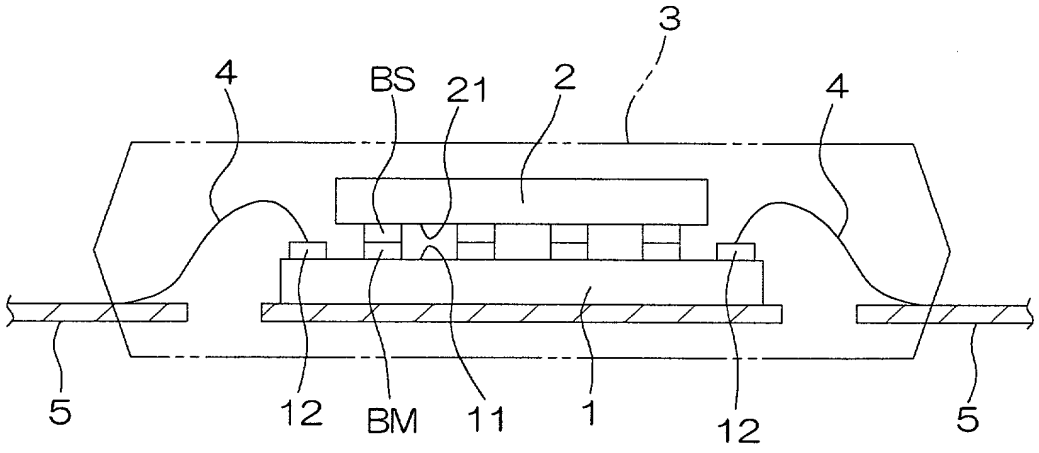
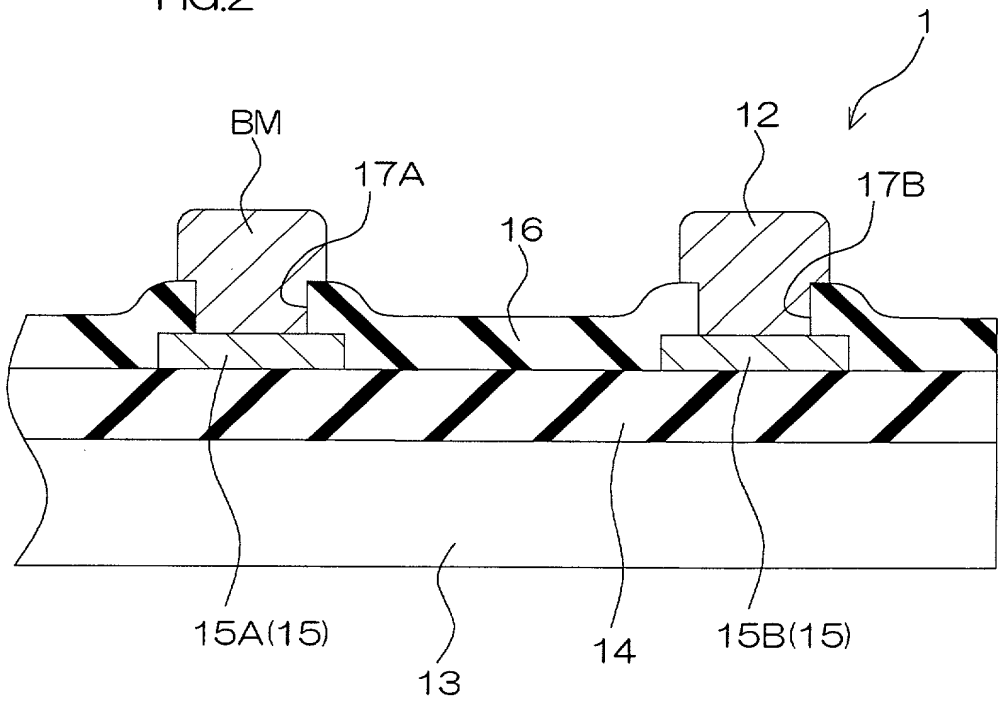


FIG.2



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Japanese Language Declaration

日本語宣言書

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下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。	I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
	SEMICONDUCTOR CHIP AND METHOD OF PRODUCING THE SAME
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Prior Foreign Application(s) 外国での先行出願			Priority Claimed 優先権主張	
11-265744	Japan	20/09/1999	☒ Yes はい	☐ No いいえ
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)		
			☐ Yes はい	☐ No いいえ
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(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (*list name and registration number*).

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第二共同発明者	Full name of second joint inventor, if any
第二共同発明者の署名 日付	Second inventor's signature Date
住所	Residence
国籍	Citizenship
私書箱	Post Office Address

（第三以降の共同発明者についても同様に記載し、署名をすること）

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